# Alex Hornung

CPU Microarchitect • Digital Design Engineer Cambridge, United Kingdom

#### About me

Experienced memory system architect with strong background in load/store design, all levels of CPU caches, data prefetching, and cache coherency.

Strong track record in all areas of IP design, from exploration and specification to RTL design, physical implementation and design verification.

Strong software development and debugging skills (C, C++, Clojure, Python, Go) from low-level microcontroller firmware and operating systems to web applications.

#### Work Experience

<ul> <li>ARM Limited</li> <li>[Senior Principal Engineer, Principal Engineer]</li> <li>Lead memory system and MMU architect for AF</li> <li>Contributor to AMBA 5 CHI coherent interconn</li> <li>Technical assessor for previous, current and next</li> </ul>	ect architecture.
<ul> <li>[Staff Engineer, Senior Engineer, Engineer]</li> <li>- Exploration and design of previous generation of</li> <li>- Micro-architecture of previous generations of inst multi-threaded A-class cores.</li> </ul>	
<ul> <li>DragonFly BSD</li> <li>Developer/Committer</li> <li>Mostly kernel code in various areas, including de cryptographic components.</li> </ul>	United Kingdom 2008 - 2013 vice drivers, file systems, schedulers and
<ul> <li>ARM Limited</li> <li>CPU Design Intern</li> <li>Development of a SystemVerilog memory control</li> <li>RTL Engineer on an SMT CPU (later cancelled)</li> </ul>	
<ul> <li>Freelance</li> <li>Software Developer</li> <li>Development of Assembly/C/C++ projects incluand user- space applications for various clients.</li> </ul>	United Kingdom June 2008 - September 2012 ding FreeBSD and Windows kernel modules

## Education

- University of Southampton
  - $MSc\ System-on-Chip$ 
    - with Distinction
- University College London BEng Electronic Engineering
  - 1st Class Honours

### Languages

Southampton, United Kingdom 2011-2012

London, United Kingdom 2008-2011

English: Fluent • Spanish: Native • German: Native • French: Limited